PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

Abstract of the Disclosure

Structures and methods for programmable array type logic and/or memory with p-channel devices and asymmetrical low tunnel barrier intergate insulators are provided. The programmable array type logic and/or memory devices include p-channel non-volatile memory which has a first source/drain region and a second source/drain region separated by a p-type channel region in an n-type substrate. A floating gate opposing the p-type channel region and is separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator. The asymmetrical low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$. The floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator. And, the control gate includes a polysilicon control gate having a metal layer, having a different work function from the metal layer formed on the floating gate, formed thereon in contact with the low tunnel barrier intergate insulator.

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